CLAIMS:

1. A semiconductor device (105, 205) comprising a silicon-containing semiconductor body (110, 210) with a surface (126, 226), which semiconductor body (110, 210) is provided, near the surface thereof (126, 226), with a transistor comprising: a gate (170, 270) situated at the surface (126, 226) and having a side wall spacer (136, 138, 236) on either side of the gate, and further comprising, on either side of the gate (170, 270), a diffusion region (180, 182, 280) formed in the semiconductor body (110, 210), at least one diffusion region (180, 182, 280) being provided at the surface (126, 226) of the semiconductor body (110, 210) with a silicide (190, 192), characterized in that the silicide (190, 192) extends along the surface (126, 226) of the semiconductor body (110, 210) and continues for more than 10 nm under the side wall spacer (136, 138, 236).

2. A semiconductor device (105, 205) as claimed in claim 1, characterized in that the silicide (190, 192) contains a metal which, in the silicide formed, has a higher diffusion rate than silicon.

3. A semiconductor device (105, 205) as claimed in claim 2, characterized in that the metal (118) is selected from the group comprising nickel (Ni), platinum (Pt) and palladium (Pd) and alloys of these metals.

4. A semiconductor device (105) as claimed in claim 1, characterized in that the side wall spacer (136, 138) is L-shaped and comprises a first portion, which borders on the gate (170) and extends substantially perpendicularly with respect to the surface (126) of the semiconductor body (110), and a second portion which extends along the surface (126) of the semiconductor body (110).

5. A semiconductor device (105) as claimed in claim 4, characterized in that the second portion of the L-shaped side wall spacer (136, 138) has a thickness (D2), measured in a direction perpendicular to the surface (126) of the semiconductor body (110), of maximally 40 nm.

6. A semiconductor device (105, 205) as claimed in claim 1, characterized in that an insulating layer (115, 215) extends in the semiconductor body (110, 210) in a direction parallel to the surface (126, 226) of the semiconductor body (110, 210).

7. A semiconductor device (105) as claimed in claim 1, characterized in that the semiconductor body (110) comprises a germanium component.

8. A semiconductor device (105) as claimed in claim 1, characterized in that the semiconductor body (110) comprises a strained-silicon layer.

9. A method of manufacturing a semiconductor device (105, 205) as claimed in claim 1, comprising the steps of:

- providing a silicon-containing semiconductor body (110, 210) having a surface (126, 226) which is provided with a gate (170, 270);
- forming a side wall spacer (136, 138, 236) on either side of the gate (170, 270);
- forming a diffusion region (180, 182, 280) in the semiconductor body (110, 210) on either side of the gate (170, 270);
- carrying out an amorphization implantation (116, 216) to render the silicon of the semiconductor body (110, 210) amorphous at the surface (126, 226) of the diffusion regions (180, 182, 280),

and

converting the silicon (189, 191, 289) that has been rendered amorphous into a silicide via interaction with a metal (118),

characterized in that

for the conversion of the silicon (189, 191, 289) that has been rendered amorphous into a silicide (190) use is made of a metal (118) which has a higher diffusion rate in the silicide (190) formed than silicon.

10. A method as claimed in claim 9, characterized in that the metal (118) is selected from the group comprising nickel (Ni), Platinum (Pt) and palladium (Pd), and alloys of these metals.

11. A method as claimed in claim 9, characterized in that the amorphization implantation angle (H1, H2) is larger than 0 degrees.

12. A method as claimed in claim 9, characterized in that the side wall spacer (136, 138) is formed so as to be L-shaped, comprising a first portion, which borders on the gate (170) and extends substantially perpendicularly with respect to the surface (126) of the semiconductor body (110), and a second portion, which extends along the surface (126) of the semiconductor body (110).

13. A method as claimed in claim 12, characterized in that the second portion of the L-shaped side wall spacer (136, 138) is formed with a thickness (D2), measured in a direction perpendicular to the surface (126) of the semiconductor body (110), of maximally 40 nm.